

**PURPOSE:** This specification defines the requirements for preassembly screening and demonstration tests for electronic piece parts of the types indicated in the title below. These tests are supported by requirements of JPL Specification ZPP-2073-GEN.

**1. Screening Tests.** These test shall be conducted in the following order except as noted.

- a. **Premeasurement visual and dimensional inspection:** Per JPL Specification ZPP-2073-GEN and JPL drawing 10146848. Serialize the devices and record their date codes.
- b. **Initial Measurements:** (at room ambient temperature)
  - 1) **Dielectric withstanding voltage:** 500 V rms, 60 Hz, applied for 60+5 seconds between the windings and the case, in accordance with MIL-STD-202, Method 301.
  - 2) **Insulation resistance:** The insulation resistance of the inductor shall be measured by applying 500 Vdc for 60 +5 seconds between the winding and the case.
  - 3) **DC resistance:** (see Table I).
  - 4) **Exciting current:** Measure exciting current per Figure 3.
  - 5) **Polarity:** The polarity shall be as shown in JPL drawing 10146848. (non-measurement)
  - 6) **Turns Ratio Test:** See Table I. Input voltages shall be 5.0 V rms, 20kHz.
- c. **Thermal Shock Test:** Perform ten (10) cycles per MIL-STD-202, Method 107D except that the temperature range shall be from -20°C to +85°C. The dwell time at 25°C shall be five minutes maximum. The winding continuity shall be continuously monitored during thermal cycling as shown in Figure 1. Maximum current shall be 50 µAdc.
- d. **Second measurements:** Repeat measurements b.2) Insulation resistance, b.3) DC resistance, and b.4) Inductance.
- e. **Operational burn-in:** Parts shall be operated continuously under the conditions shown in Figure 2 for 168 +8/-0 hours at a temperature of +85°C. Voltage and temperature shall be monitored by a technician who shall record all anomalies and corrections.
- f. **Final measurements:** Repeat initial measurements and record.

<b>RELEASED THRU SECTION 356 DATA MANAGEMENT:</b>		<b>DATE:</b>	
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<b>VENDOR PART NO</b>	<b>VENDOR</b>	<b>JPL PART NO</b>	
<b>JET PROPULSION LABORATORY    CALIFORNIA INSTITUTE OF TECHNOLOGY</b>			
Procurement specification: JPL drawing 10146848 Screening specification: ZPP-2073-GEN	<b>TITLE:</b>  <b>Test Specification</b> <b>Sync Power Converter Transformer: 10146848 - T2</b> <b>WFPC II - AFM</b>		<b>JPL CAGE NO 23835</b>
			<b>ST 12180</b>
			<b>SHEET 1 OF 4</b>
Custodian: Electronic Parts Reliability Section 514			

g. Device acceptance criteria shall be as follows:

1) DC coil resistance shall remain within the tolerance limits shown in Table I.

2) Inductance shall remain within tolerance limits shown in Table I.

3) Insulation Resistance shall be 10,000 megohms minimum.

4) The winding shall exhibit no discontinuities during thermal cycling.

5) Second measurements: Percent change from initial measurement shall not exceed the amount specified in Table I.

6) Final measurements: Percent change from initial measurement shall not exceed the amount specified in Table I.

7) Dielectric withstanding voltage test shall cause no evidence of arcing, flashover, breakdown of insulation, or damage.

2. **Demonstration Tests.** Demonstration tests are waived for the WFPC II Articulating Folding Mirror (AFM) electronic parts, including magnetic devices (reference IOM 700/RLH - AFM Compliance Matrix). Subsequently, this section does not apply to the devices indicated in the title of this specification.

TABLE I. Electrical Characteristics

Parameter	Limits	Maximum Deviation From Initial Measurement	
		Second Measurement	Final Measurement
Dielectric strength	No breakdown or arcing		No breakdown or arcing
Insulation Resistance	10 k megohms minimum	10 k megohms minimum	10 k megohms minimum
Turns Ratio Test	Tolerance $\pm 3\%$		$\pm 1\%$
1-2 : 5-6	0.021		
3-4 : 5-6	0.021		
7-8 : 5-6	0.750		
DC Resistance		$\pm 5\%$	$\pm 5\%$
1-2	0.001 $\Omega$ maximum		
3-4	0.001 $\Omega$ maximum		
5-6	0.11 $\Omega$ maximum		
7-8	0.74 $\Omega$ maximum		

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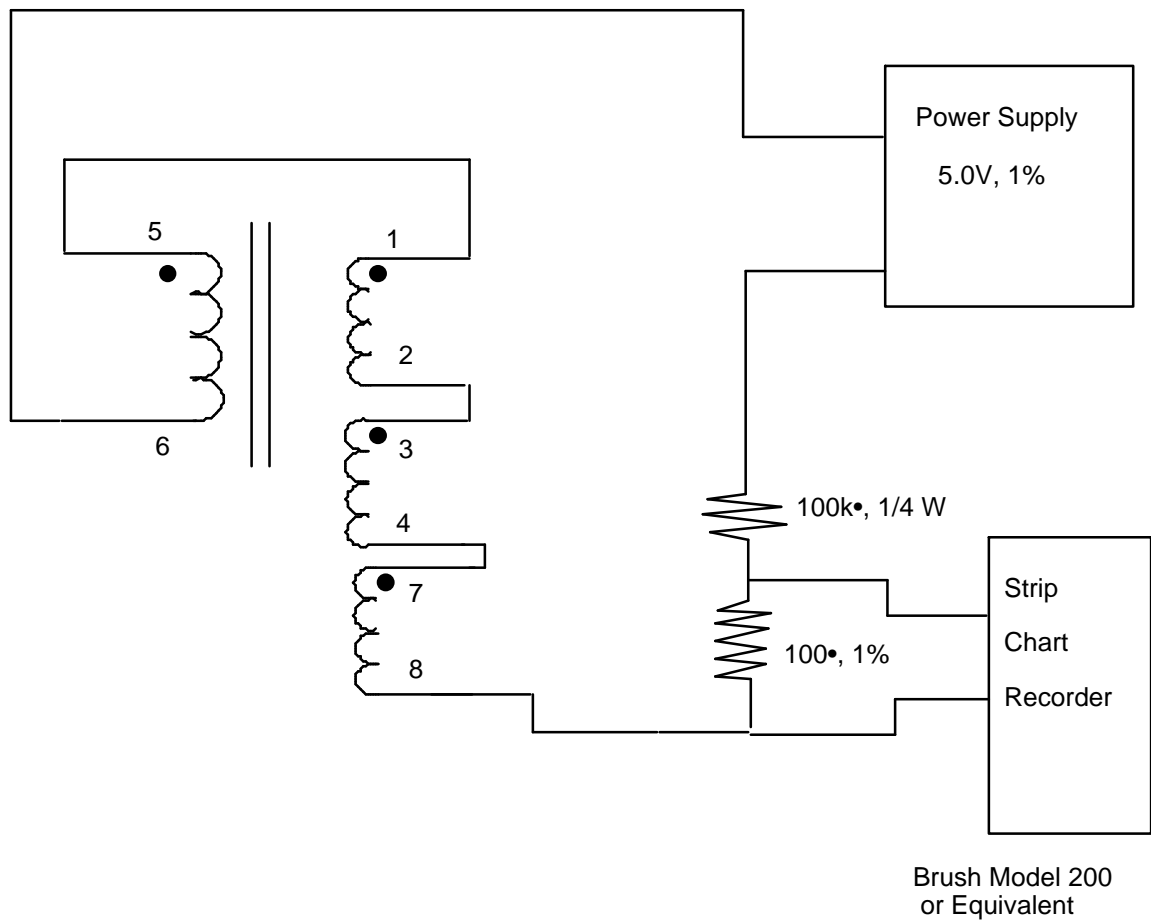


Figure 1. Continuity Monitor Circuit

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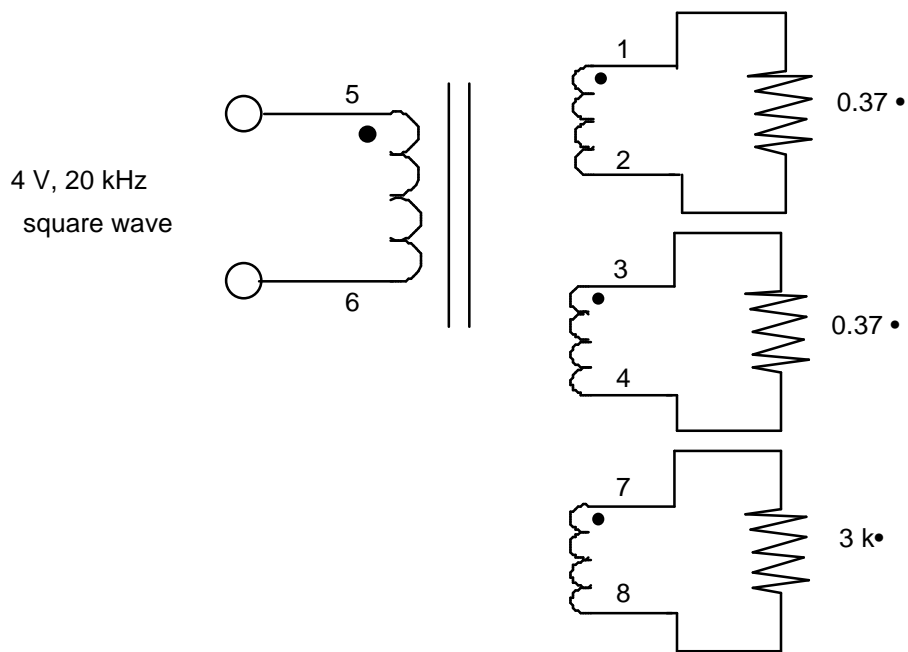


Figure 2. Burn-in Circuit

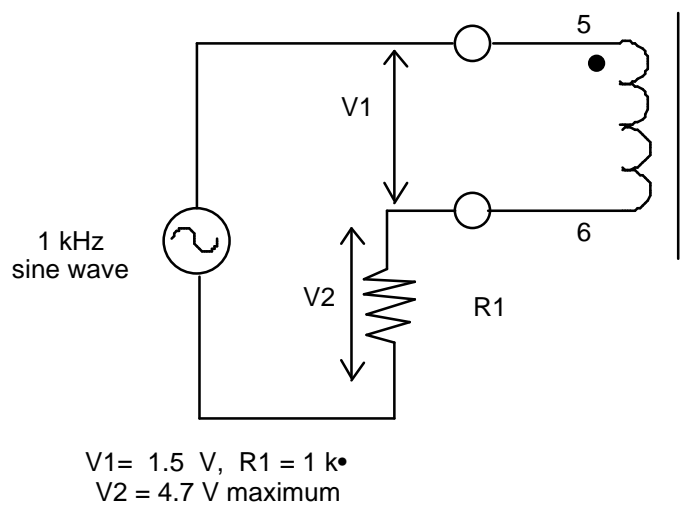


Figure 3. Exciting Current Test Circuit

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